WHAT IS CLAIMED IS:

1. A nonvolatile memory comprising:

a memory cell array including a plurality of memory cells being formed in a matrix;

each of the memory cells including a memory thin film transistor and a switching thin film transistor;

said memory thin film transistor including:

a first semiconductor active layer over an insulating substrate;

a first insulating film;

a floating gate electrode;

a second insulating film;

a control gate electrode;

said switching thin film transistor including:

a second semiconductor active layer over the insulating substrate;

a gate insulating film;

a gate electrode,

wherein the memory thin film transistor and the switching thin film transistor are integrally formed over the insulating substrate,

wherein the first semiconductor active layer of the memory thin film transistor and the second semiconductor active layer are continuously formed,

wherein a first thickness of the first semiconductor active layer of the memory thin film transistor is thinner than a second thickness of the second semiconductor active layer of the switching thin film transistor.

2. A memory according to claim 1,

wherein each of the first and second thicknesses is in a range of 1-150 nm.

3. A nonvolatile memory comprising:

a memory cell array including a plurality of memory cells being formed in a matrix;

each of the memory cells including a memory thin film transistor and a switching thin film transistor;

said memory thin film transistor including:

a first semiconductor active layer over an insulating substrate;

a first insulating film;

a floating gate electrode;

a second insulating film;

a control gate electrode;

said switching thin film transistor including:

a second semiconductor active layer over the insulating substrate;

a gate insulating film;

a gate electrode,

wherein the memory thin film transistor and the switching thin film transistor are integrally formed over the insulating substrate,

wherein the first semiconductor active layer of the memory thin film transistor and the second semiconductor active layer are continuously formed,

wherein a first thickness of the first semiconductor active layer of the memory thin film transistor is in a range of 1-100 nm while a second thickness of the second semiconductor active layer of the switching thin film transistor is in a range of 1-150 nm.

4. A memory according to claim 1,

wherein the first thickness in a range of 1-50 nm while the second thickness is in a range of 10-100 nm.

5. A memory according to claim 4,

wherein the first thickness is in a range of 10-40 nm.

6. A memory according to claim 1,

wherein the first thickness of the first semiconductor active layer of the memory thin film transistor is more likely to cause impact ionization than the second thickness of the second semiconductor active layer.

7. A memory according to claim 1,

wherein a first tunnel current flowing between the floating gate electrode and the first semiconductor active layer of the memory thin film transistor is twice or more of a second tunnel current flowing between the gate electrode and the second semiconductor active layer of the switching thin film transistor.

8. A memory according to claim 1,

wherein each of the memory thin film transistor and the switching thin film transistor is a p-channel thin film transistor.

9. A memory according to claim 1, further comprising a driver circuit for driving the plurality of memory cells,

wherein the memory cell array and the driver circuit are integrally formed over the insulating substrate.

10. A semiconductor device including the nonvolatile memory of claim 1, said semiconductor device further comprising:

a pixel portion;

a driver circuit for driving the pixel portion,

wherein the pixel portion, the driver portion and the nonvolatile memory are integrally formed over the insulating substrate.

11. A device according to claim 10,

wherein the semiconductor device is one selected from the group consisting of a liquid crystal display device and an EL display device.

12. A device according to claim 10,

wherein the semiconductor device is one selected from the group consisting of a display, a video camera, a head-mounted type display, a DVD display, a goggle type display, a personal computer, a portable telephone, and a car audio.

13. A method of manufacturing a nonvolatile memory,

said nonvolatile memory including a memory cell array having a plurality of memory cells being formed in a matrix,

each of said plurality of memory cells including a memory thin film transistor and a switching thin film transistor,

said method comprising the steps of:

forming a first amorphous semiconductor layer and a second amorphous semiconductor layer over an insulating substrate;

crystallizing the first amorphous semiconductor layer and the second amorphous semiconductor layer to form a crystalline semiconductor layer having a first region with a first thickness and a second region with a second thickness;

forming the memory thin film transistor including the first region with the first thickness as a first semiconductor active layer;

forming the switching thin film transistor including the second region with the second thickness as a second semiconductor active layer,

wherein the first thickness is thinner than the second thickness.

14. A method according to claim 13,

wherein each of the first and second thicknesses is in a range of 1-150 nm.

15. A method of manufacturing a nonvolatile memory,

said nonvolatile memory including a memory cell array having a plurality of memory cells being formed in a matrix,

each of said plurality of memory cells including a memory thin film transistor and a switching thin film transistor,

said method comprising the steps of:

forming a first amorphous semiconductor layer and a second amorphous semiconductor layer over an insulating substrate;

crystallizing the first amorphous semiconductor layer and the second amorphous semiconductor layer to form a crystalline semiconductor layer having a first region with a first thickness and a second region with a second thickness;

forming the memory thin film transistor including the first region with the first thickness as a first semiconductor active layer;

forming the switching thin film transistor including the second region with the second thickness as a second semiconductor active layer,

wherein a first thickness of the first semiconductor active layer of the memory thin film transistor is in a range of 1-100 nm while a second thickness of the second semiconductor active layer of the switching thin film transistor is in a range of 1-150 nm.

16. A method according to claim 13,

wherein the first thickness in a range of 1-50 nm while the second thickness

is in a range of 10-100 nm.

17. A method according to claim 16,

wherein the first thickness is in a range of 10-40 nm.

18. A method according to claim 13,

wherein the first thickness of the first semiconductor active layer of the memory thin film transistor is more likely to cause impact ionization than the second thickness of the second semiconductor active layer.

19. A method according to claim 13,

wherein a first tunnel current flowing between the floating gate electrode and the first semiconductor active layer of the memory thin film transistor is twice or more of a second tunnel current flowing between the gate electrode and the second semiconductor active layer of the switching thin film transistor.

20. A method according to claim 13,

wherein each of the memory thin film transistor and the switching thin film transistor is a p-channel thin film transistor.

21. A method according to claim 13,

wherein the nonvolatile memory further comprises a driver circuit for driving the plurality of memory cells,

wherein the memory cell array and the driver circuit are integrally formed over the insulating substrate.

22. A method of fabricating a semiconductor device including the nonvolatile

memory being manufactured by the method of claim 13,

said semiconductor device further comprising:

a pixel portion;

a driver circuit for driving the pixel portion;

wherein the pixel portion, the driver portion and the nonvolatile memory are integrally formed over the insulating substrate.

23. A method according to claim 22,

wherein the semiconductor device is one selected from the group consisting of a liquid crystal display device and an EL display device.

24. A method according to claim 22,

wherein the semiconductor device is one selected from the group consisting of a display, a video camera, a head-mounted type display, a DVD display, a goggle type display, a personal computer, a portable telephone, and a car audio.

25. A method according to claim 15,

wherein the first thickness in a range of 1-50 nm while the second thickness is in a range of 10-100 nm.

26. A method according to claim 25,

wherein the first thickness is in a range of 10-40 nm.

27. A method according to claim 15,

wherein the first thickness of the first semiconductor active layer of the memory thin film transistor is more likely to cause impact ionization than the second thickness of the second semiconductor active layer.

28. A method according to claim 15,

wherein a first tunnel current flowing between the floating gate electrode and the first semiconductor active layer of the memory thin film transistor is twice or more of a second tunnel current flowing between the gate electrode and the second semiconductor active layer of the switching thin film transistor.

29. A method according to claim 15,

wherein each of the memory thin film transistor and the switching thin film transistor is a p-channel thin film transistor.

30. A method according to claim 15,

wherein the nonvolatile memory further comprises a driver circuit for driving the plurality of memory cells,

wherein the memory cell array and the driver circuit are integrally formed over the insulating substrate.

31. A method of fabricating a semiconductor device including the nonvolatile memory being manufactured by the method of claim 15,

said semiconductor device further comprising:

a pixel portion;

a driver circuit for driving the pixel portion;

wherein the pixel portion, the driver portion and the nonvolatile memory are integrally formed over the insulating substrate.

32. A method according to claim 31,

wherein the semiconductor device is one selected from the group consisting of a liquid crystal display device and an EL display device.

33. A method according to claim 31,

wherein the semiconductor device is one selected from the group consisting of a display, a video camera, a head-mounted type display, a DVD display, a goggle type display, a personal computer, a portable telephone, and a car audio.

34. A memory according to claim 3,

wherein the first thickness in a range of 1-50 nm while the second thickness is in a range of 10-100 nm.

35. A memory according to claim 34,

wherein the first thickness is in a range of 10-40 nm.

36. A memory according to claim 3,

wherein the first thickness of the first semiconductor active layer of the memory thin film transistor is more likely to cause impact ionization than the second thickness of the second semiconductor active layer.

37. A memory according to claim 3,

wherein a first tunnel current flowing between the floating gate electrode and the first semiconductor active layer of the memory thin film transistor is twice or more of a second tunnel current flowing between the gate electrode and the second semiconductor active layer of the switching thin film transistor.

38. A memory according to claim 3,

wherein each of the memory thin film transistor and the switching thin film transistor is a p-channel thin film transistor.

39. A memory according to claim 3, further comprising a driver circuit for driving the plurality of memory cells,

wherein the memory cell array and the driver circuit are integrally formed over the insulating substrate.

40. A semiconductor device including the nonvolatile memory of claim 3, said semiconductor device further comprising:

a pixel portion;

a driver circuit for driving the pixel portion,

wherein the pixel portion, the driver portion and the nonvolatile memory are integrally formed over the insulating substrate.

41. A device according to claim 40,

wherein the semiconductor device is one selected from the group consisting of a liquid crystal display device and an EL display device.

42. A device according to claim 40,

wherein the semiconductor device is one selected from the group consisting of a display, a video camera, a head-mounted type display, a DVD display, a goggle type display, a personal computer, a portable telephone, and a car audio.